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MERED, HABTE	

ART UNIT	PAPER NUMBER
2662	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/916,406	KHANKHEL, SAEEDA	
	Examiner	Art Unit	
	Habte Mered	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 27 July 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 20050308.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-9 and 22-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US 4, 516, 238), hereinafter referred to as Huang, in view of Cooperman et al (US 5, 862, 128), hereinafter referred to as Cooperman.

3. Regarding **claim 1**, Huang teaches a full access, non-blocking, wide band switching system in Figure 1 that is designed to switch signals that have destination addresses embedded in the signal structure. The system of figure 1 comprises of a concentrator, a self-routing sorting network, a trap network, and a self –routing expander.

Huang further discloses a switching system for a telecommunications network, comprising:

a) a first stage having input and output sides, where the output side is concentrated relative to the input side **(See Column 5, Lines 7-11 and Lines 35-48;)**; and

b) a second stage having input and output sides, where the input side of the second stage is coupled to the output side of the first stage and the output side of the second stage being comprised of a plurality of outputs **(See Column 5, Lines 10-14; Huang discloses that the first stage (i.e. concentrator) outputs collectively labeled as 1100 in Figure 1 is the input to the second stage and the second stage can be viewed as a stage that includes the sorter sub-network and the optional trap sub-network.)**

Huang, however, fails to teach aging each cell having a non-unique destination address in the second stage.

Cooperman teaches a system that improves existing switching architectures like that of Huang's by replacing the trap sub-network with a merged buffer architecture as shown in Figure 5. Cooperman further discloses when a plurality of cells arrive, at the second stage, in a first time slot, then the second stage places each cell having a unique destination address on one of the selected plurality of outputs and ages each cell having a non-unique destination address. **(See Column 3, Lines 20-55; Cooperman discloses that the circuit switch matrix sorts the input signal based on the output port destination. The circuit switch matrix in effect is Huang's sorter sub-network that is part of the second stage. Based on the applicant's definition found on page 11 of the specification, a non-unique destination address occurs when more than one cell have the same destination address in a given time slot which necessitates output contention. Cooperman teaches that if more than one input signal is contending, for an output port, the second stage**

(i.e. circuit switch matrix plus the merged buffer architecture) ages the cells having non-unique address by misrouting them intentionally to a merged buffer that is not busy. The second stage does not reroute a misrouted signal until the second half of a time slot when the intended buffer is not busy.)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a merged buffer architecture to age cells causing output contention by having same destination address in the same time slot. The motivation to add the merged buffer architecture is to decrease excessive latency that could cause loss of signal integrity. The continuous re-circulation of contending signals without checking the buffer status causes the excessive latency.

4. Regarding **claim 2** the modified invention of Huang and Cooperman as taught above disclosed the aforementioned invention including the first stage in Huang's switching system shown in Figure 1 is a concentrator. **(See Element 10 in Figure 1; Column 5, Lines 5-7)**

5. Regarding **claim 3**, the modified invention of Huang and Cooperman as taught above disclosed the aforementioned invention including the first stage in Huang's switching system shown in Figure 1 is a concentrator and performs an N: L concentration on cells arriving in the first time slots. **(See Element 10 in Figure 1; Column 5, Lines 6-11 and Lines 34-52; Huang explains the need for a concentrator and shows why when having N input signals at the concentrator where only L of the non-adjacent N input signals are active at a time the output of**

the concentrator will be L adjacent active output signals where the non-active input signals are dropped and L < N)

6. Regarding **claim 4**, Huang shows in Figure 1 that the output of the concentrator (element 10) is fed to the sorting sub-network **(element 20 in Figure 1)**, which in turn is connected to the trapping network **(element 30 in Figure 1)**. The sorting sub-network and the trapping network can be viewed as one stage.

Huang, however, fails to teach that the second stage can be a non-re-circulating sort and trap stage.

Cooperman teaches a system that improves existing switching architectures like that of Huang's by replacing the trap sub-network with a merged buffer architecture as shown in Figure 5. Since Cooperman's merged buffer architecture is non-circulating it constitutes a non-re-circulating sort and trap stage. **(See Column 2, Lines 48-56 and 60-65; Column 6, Lines 56-66; Cooperman teaches the disadvantage of re-circulating cells that can cause output contention and uses a temporary delay until the output port is no longer busy before routing the cells to the correct destination.)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a non-circulating merged buffer architecture to age cells causing output contention by having same destination address in the same time slot. The motivation to add the non-circulating merged buffer architecture is to decrease excessive latency that could cause loss of

signal integrity. The continuous re-circulation of contending signals without checking the buffer status causes the excessive latency.

7. Regarding **claims 5, 8 and 22**, Huang discloses a switching system that has a second stage that comprises a sorter sub-stage for arranging the plurality of cells arriving at the second stage in a first time slot in a first order, where the first order is based upon the destination address. **(See Column 7, Lines 55-64 and Column 8, Lines 10-24; It is important to note that the combination of the sorter and trap networks can be viewed as constituting the second stage of Huang's switching system)**

Huang, however, fails to disclose that the second stage needs to take into consideration the priority assigned to the incoming cells as well as aging cells causing contention problems with non-unique destination address.

Cooperman teaches that incoming cells are sorted and eventually routed to the appropriate output ports after taking into consideration the destination address and priority assigned to each of them. **(See Column 3, Lines 1-3 and 49-55; Column 4, Lines 27-32; and Column 5, Lines 8-24)** Cooperman teaches a multi-cast switching **(See Cooperman Column 9, Line 11 and Figure 9)** system that improves existing switching architectures like that of Huang's by replacing the trap sub-network with a merged buffer architecture as shown in Figure 5. Cooperman's switching system routes each cell having a unique destination address to the appropriate output while aging each cell having a non-unique address. In Cooperman's switching system the aged

cells with non-unique destination address are routed in the next time slot. **(Cooperman teaches the immediate routing of cells with unique destination address to a non-busy output port in Figure 7 which is the case with cell 1 having a unique address of output 3 and is being routed to output 3 in the same time slot. As shown in Figure 7, cells 2 and 3 have a non-unique address of output 1 and consequently cell 1 is routed to output 1 and cell 2 is aged by misrouting it to a non-busy merged buffer. Cell 2 is then routed to buffer 1 in the second part of the first time slot and in the first part of the next time slot cell 2 is routed to output 1. Cell 2 was successfully routed to output 1 because the destination address of cell 2 is no longer non-unique and there is no output contention. See Column 7, Lines 29-62).**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a merged buffer architecture to age cells causing output contention by having same destination address in the same time slot. The motivation to add the merged buffer architecture is to decrease excessive latency that could cause loss of signal integrity. The continuous re-circulation of contending signals without checking the buffer status causes the excessive latency.

8. Regarding **claim 6**, both Huang and Cooperman teach the aforementioned invention, including the sorter sub-stage being a Batcher sorter. **(See Huang Column 7, Lines 65-68 and Cooperman Column 5, Lines 10-15)**

9. Regarding **claim 7**, Huang disclosed the aforementioned invention but does not disclose a trap buffer in which cells having non-unique destination addresses for the first time are aged until the next time slot.

In Cooperman's switching system the aged cells with non-unique destination address are routed in the next time slot. (**See Column 6, Lines 56-62; Column 7, Lines 29-62; It is important to note that Cooperman uses the merged output buffer for two distinct purposes. First, the merged output buffer serves as the output of the second stage and therefore serves as the logical output buffer for the correctly routed cells with unique destination address. Second, the non-busy part of the merged buffer really serves as "trap buffer", for the cells with non-unique destination addresses that are eventually misrouted. In Figure 7, cells 2 and 3 have a non-unique address of output 1 and consequently cell 1 is routed to output 1 and cell 2 is aged by misrouting it to a non-busy merged buffer. Cell 2 is then routed to buffer 1 in the second part of the first time slot and in the first part of the next time slot cell 2 is routed to output 1. Cell 2 was successfully routed to output 1 because the destination address of cell 2 is no longer non-unique and there is no output contention.)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a merged buffer architecture to age cells causing output contention by having same destination address in the same time slot. The motivation to add the merged buffer architecture is to decrease excessive latency that could cause loss of signal integrity. The continuous re-

circulation of contending signals without checking the buffer status causes the excessive latency.

10. Regarding **claims 9 and 23**, the modified invention of Huang and Cooperman as taught above disclosed the aforementioned invention including:

a) a third stage having an input side comprised of a plurality of inputs, each input coupled to a corresponding one of the plurality of outputs of the second stage (**See Huang Column 5, Lines 18-29; Element 40 in Figure 1 and Figures 13-15.)**

b) wherein, in the first time slot and each one of a series of at least one subsequent time slots, the second stage placing a cell having a unique destination address on one of the plurality of outputs **(See Cooperman Column 3 Lines 23-34; Column 6, Lines 56-60; Column 7, Lines 30-60; Cooperman discloses the merged buffers act as a logical outlook buffer for correctly routed cells (i.e. those with unique destination addresses) and explains further that in every single time slot these cells with unique destination address (e.g. cell 1 in Figure 7) are placed at the output of the second stage)**

c) that the system can be a multi-cast switching system **(See Cooperman Column 9, Line 11 and Figure 9)**

11. **Claims 10-11 and 24-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US 4, 516, 238), hereinafter referred to as Huang, in view of Cooperman et al (US 5, 862, 128), hereinafter referred to as Cooperman, as applied to claims 1, 8 and 9 above, and further in view of Widjaja et al (US 5, 440, 553), hereinafter referred to as Widjaja.

12. Regarding **claims 10 and 24**, the modified invention of Huang and Cooperman as taught above disclosed the aforementioned invention including that the switch can be a multi-cast switching system **(See Cooperman Column 9, Line 11 and Figure 9)**. However the modified invention of Huang and Cooperman fails to teach that the third stage of the switch can comprise a queuing stage.

Widjaja teaches an output buffered packet multi-stage switch (See Figures 3 and 4) with priority packet transmission and flexible buffer management scheme. The switch in Figure 3 has a sorter and trap sub-stages and the output of the sorter and trap stage is fed to a queuing stage as shown in Figures 1a and 1b. **(See Column 3, Lines 63-68 and Column 4, Lines 1-9).**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the modified invention of Huang's and Cooperman's switching system by incorporating a queuing stage, the motivation being achieving buffer efficiency while avoiding any potential lockout problem.

13. Regarding **claims 11 and 25**, the modified invention of Huang and Cooperman as taught above disclosed the aforementioned invention including that the switch can be a multi-cast switching system **(See Cooperman Column 9, Line 11 and Figure 9)** but does not disclose that the queuing stage has a plurality of queues that matches the number of outputs of the switching system.

Widjaja teaches an output buffered packet multi-stage switch wherein the queuing stage further comprises a plurality of queues, each having an input coupled to a corresponding one of the plurality of outputs of the second stage and system output;

each one of the plurality of queues buffering cells having a common destination address to be output by the switching system. **(See Column 3, Lines 63-68 and Column 4, Lines 1-9; Figures 1a and 1b).**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the modified invention of Huang's and Cooperman's switching system by incorporating a queuing stage, the motivation being achieving buffer efficiency while avoiding any potential lockout problem.

14. **Claims 12-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US 4, 516, 238), hereinafter referred to as Huang, in view of Cooperman et al (US 5, 862, 128), hereinafter referred to as Cooperman, and Widjaja et al (US 5, 440, 553), hereinafter referred to as Widjaja.

15. Regarding **claim 12**, Huang discloses a high performance switching system, comprising of a concentrator stage having a plurality of input ports for the switching system and a plurality of outputs, where the concentrator concentrates cells entering the switch on the plurality of input ports and then routes the concentrated cells onto the plurality of outputs by discarding idle ones of the plurality of inputs **(See Huang Column 5, Lines 5-11 and Lines 35-48; See Element 10 in Figure 1)**.

Huang fails to disclose that the switching system can have a non-re-circulating Batcher-sorter and trap stage. Huang fails to disclose that his switching system can have a queuing system as well as serve ATM platform.

Cooperman teaches that an ATM switching system **(Cooperman Column 7, Line 33)** can have a non-re-circulating Batcher-sorter and trap stage having a plurality

of inputs and a plurality of outputs, each of the plurality of inputs of the non-re-circulating Batcher sorter trap stage coupled to a corresponding one of the plurality of outputs of the concentrator stage **(See Huang Column 5, Lines 10-14; Huang discloses that the first stage (i.e. concentrator) outputs collectively labeled as 1100 in Figure 1 is the input to the second stage. The second stage can be viewed as a stage that includes the sorter sub-network and the optional trap sub-network. Cooperman teaches a system that improves existing switching architectures like that of Huang's by replacing the trap sub-network with a merged buffer architecture as shown in Figure 5. Since in Cooperman's merged buffer architecture the aged cell is not re-circulated it constitutes a non-re-circulating sort and trap stage. See Cooperman Column 2, Lines 48-56 and 60-65; Cooperman Column 6, Lines 56-66; Cooperman teaches the disadvantage of re-circulating cells and uses a temporary delay until the output port is no longer busy before routing the cells to the correct destination.)**

Cooperman also teaches that the non-re-circulating Batcher-sorter and trap stage places, cells arriving at its input during any given time slot, are routed to its corresponding output in the same given time slot provided that the cells arriving at the input have a unique address. **(Cooperman teaches the immediate routing (i.e. the same time slot) of cells with unique destination address to a non-busy output port in Figure 7 which is the case with cell 1 having a unique address of output 3 and is being routed to output 3 in the same time slot. See Cooperman Column 7, Lines 29-62 and Cooperman Column 3 Lines 28-34)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a non-circulating merged buffer architecture to age cells causing output contention by having the same destination address in the same time slot. The motivation to add the non-circulating merged buffer architecture is to decrease excessive latency that could cause loss of signal integrity. The continuous re-circulation of contending signals without checking the buffer status causes the excessive latency.

Huang and Cooperman fail to disclose that the modified switching system invention can have a third stage where the third stage is a queuing stage.

Widjaja teaches an output buffered packet multi-stage switch (See Figures 3 and 4) with priority packet transmission and flexible buffer management scheme. Widaja discloses that the switching system has a plurality of queues and each one of the queues have an input coupled to a corresponding one of the plurality of outputs of the non-re-circulating Batcher sorter trap stage and an output port for the switching system, and each one of the plurality of queues buffers cells exiting the switching system which share a common destination address **(See Widjaja Column 3, Lines 63-68 and Widjaja Column 4, Lines 1-9; Figures 1a and 1b)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the modified invention of Huang's and Cooperman's switching system by incorporating a queuing stage, the motivation being achieving buffer efficiency while avoiding any potential lockout problem.

16. Regarding **claim 13**, the modified invention of Huang, Cooperman, and Widjaja as taught above disclosed the aforementioned invention including a switching system of wherein the non-re-circulating Batcher sorter trap stage further comprises:

a) a sorter sub-stage for ordering the plurality of cells arriving at the second stage in each one of the plurality of time slots based upon the destination address and a priority for each one of the plurality of arriving cells; **(See Cooperman Column 3, Lines 1-3 and 49-55; Cooperman Column 4, Lines 27-32; and Cooperman Column 5, Lines 8-24)** and

b) a trap substage for placing, during each one of the plurality of time slots, each one of the plurality of cells having either a unique destination address or the highest priority among cells sharing a non-unique destination address on a selected one of the plurality of outputs **(See Cooperman Column 7, Lines 29-62 and Cooperman Column 3 Lines 28-34)**;

c) for each one of the plurality of time slots, the trap substage selecting cells for placement on the plurality of outputs from a set of cells comprised of cells arriving from said sorter substage during that one of the plurality of time slots and cells aged from the time slot immediately preceding that one of the current plurality of time slots(**In Figure 7, cells 2 and 3 have a non-unique address of output 1 and consequently cell 1 is routed to output 1 and cell 2 is aged by misrouting it to a non-busy merged buffer. Cell 2 is then routed to buffer 1 in the second part of the first time slot and in the first part of the next time slot cell 2 is routed to output 1. Cell 2 was successfully routed to output 1 because the destination address of cell 2 is no**

longer non-unique and there is no output contention. See Cooperman Column 7, Lines 29-62).

17. Regarding **claim 14**, the modified invention of Huang, Cooperman, and Widjaja as taught above disclosed the aforementioned invention including a switching system of wherein the concentrator stage performs N:L concentrations on arriving cells. **(See Element 10 in Figure 1; Column 5, Lines 6-11 and Lines 34-52; Huang explains the need for a concentrator and shows why when having N input signals at the concentrator where only L of the non-adjacent N input signals are active at a time the output of the concentrator will be L adjacent active output signals where the non-active input signals are dropped and L < N)**

18. Regarding **claim 15**, the modified invention of Huang, Cooperman, and Widjaja as taught above disclosed the aforementioned invention including a switching system of wherein the sorter sub-stage is a Batcher sorter. **(Both Huang and Cooperman teach the aforementioned invention, including the sorter sub-stage being a Batcher sorter. Huang Column 7, Lines 65-68 and Cooperman Column 5, Lines 10-15)**

19. Regarding **claim 16**, the modified invention of Huang, Cooperman, and Widjaja as taught above disclosed the aforementioned invention including a switching system of wherein the trap sub-stage further comprises a trap buffer for aging cells with non-unique address. **(See Cooperman Column 6, Lines 56-62; Cooperman Column 7, Lines 29-62; It is important to note that Cooperman uses the merged output buffer for two distinct purposes. First, the merged output buffer serves as the output of the second stage and therefore serves as the logical output buffer for the**

correctly routed cells with unique destination address. Second, the non-busy part of the merged buffer really serves as "trap buffer", for the cells with non-unique destination addresses that are eventually misrouted. In Figure 7, cells 2 and 3 have a non-unique address of output 1 and consequently cell 1 is routed to output 1 and cell 2 is aged by misrouting it to a non-busy merged buffer. Cell 2 is then routed to buffer 1 in the second part of the first time slot and in the first part of the next time slot cell 2 is routed to output 1. Cell 2 was successfully routed to output 1 because the destination address of cell 2 is no longer non-unique and there is no output contention.).

20. **Claims 17-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US 4, 542, 497), hereinafter referred to as A. Huang, in view of Cooperman et al (US 5, 862, 128), hereinafter referred to as Cooperman.

21. Regarding **claim 17**, A. Huang discloses a multi-cast switching system in Figure 6 that has a broadcast network stage consisting of source sorting sub-stage and copy sub-stage. The source sorting sub-stage, which is element 4 in Figure 6, sorts incoming cells on the source address and feeds it to the copy sub-stage, which is element 42 in Figure 6. Thus, at the outputs of the sorting network, the original cells and the associated empty copy cells with the same source address appear contiguously. The copy sub-stage then replicates the data in each source cell and inserts this data into the data fields of the associated empty copy cells. **(See A. Huang Column 3, Lines 25-50)**

The multi-cast switching system disclosed by A. Huang, comprises a broadcast network having input and output sides, the broadcast network receives, on its input side,

a plurality of source cells from at least one source and a plurality of empty copy cells, the broadcast network copies data from selected ones of the plurality of source cells and inserts this data in the empty copy cells to produce copies of the source cells **(See A. Huang Column 9, Lines 35-55 and Column 11, Lines 5-10)**

A. Huang discloses that the inputs to the broadcast network consisting of the source sorting and copying sub-stages are source and empty copy cells. **(See A. Huang Column 3, Lines 25-50 and Column 9, Lines 35-55)**

A. Huang fails to teach a switching system with a non-circulating Batcher sort-trap stage.

Cooperman teaches a multi-cast switching system **(See Cooperman Column 9, Line 11 and Figure 9)** that has a non-re-circulating Batcher sort-trap stage having input and output sides, where the input side of the non-re-circulating Batcher sort-trap stage (i.e. second stage) is coupled to the output side of the broadcast network and the output side of the second stage comprises of a plurality of outputs. **(See A. Huang Column 9, Lines 29-35 and Column 10, Lines 26-34; A. Huang's Figure 6; A. Huang discloses that the first stage output (i.e. broadcast network, element 40, in A. Huang Figure 6) is connected to a second stage. The second stage can be viewed as a stage that includes the sorter on destination sub-network and the optional trap sub-network. Cooperman teaches a system that improves existing switching architectures like that of A. Huang's by replacing the trap sub-network with a merged buffer architecture as shown in Cooperman's Figure 5. Since in Cooperman's merged buffer architecture the aged cell is not re-circulated it**

constitutes a non-re-circulating sort and trap stage. See Cooperman Column 2, Lines 48-56 and 60-65; Cooperman Column 6, Lines 56-66; Cooperman teaches the disadvantage of re-circulating cells and uses a temporary delay until the output port is no longer busy before routing the cells to the correct destination.)

Cooperman also teaches that the non-re-circulating Batcher-sorter and trap stage places, cells arriving at its input during any given time slot, are routed to its corresponding output in the same given time slot provided that the cells arriving at the input have a unique address. **(Cooperman teaches the immediate routing (i.e. the same time slot) of cells with unique destination address to a non-busy output port in Figure 7 which is the case with cell 1 having a unique address of output 3 and is being routed to output 3 in the same time slot. See Cooperman Column 7, Lines 29-62 and Cooperman Column 3 Lines 28-34)**

In Cooperman's switching system cells with non-unique destination address are aged and routed in the next time slot. (**See Column 6, Lines 56-62 and Column 7, Lines 29-62;)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify A. Huang's switching system to incorporate a non-circulating merged buffer architecture to age cells causing output contention by having the same destination address in the same time slot. The motivation to add the non-circulating merged buffer architecture is to decrease excessive latency that could cause loss of signal integrity. The continuous re-circulation of contending signals without checking the buffer status causes the excessive latency.

22. Regarding **claim 18**, the modified invention of A. Huang and Cooperman as taught above disclosed the aforementioned invention including a multi-cast switching system wherein the broadcast network further comprises:

a) a source sort stage for sorting source and copy packets entering the source sort stage based upon a data source identifier for each one of the plurality of source packets and the plurality of copy packets **(See A. Huang Column 10, Lines 57-65)**; and

b) a copy stage for copying data from source packets containing a first data source identifier to copy packets containing the first data source identifier. **(See A. Huang Column 11, lines 5-10)**

23. Regarding **claim 19**, the modified invention of A. Huang and Cooperman as taught above disclosed the aforementioned invention including a multi-cast switching system wherein the non-recirculating Batcher sort-trap stage further comprises:

a) a sorter for arranging a plurality of cells arriving at the second stage in the first time slot in a first order where the first order is based on destination address and priority for each arriving cell; **(Cooperman teaches that incoming cells are sorted and eventually routed to the appropriate output ports after taking into consideration the destination address and priority assigned to each of them. See Column 3, Lines 1-3 and 49-55; Column 4, Lines 27-32; and Column 5, Lines 8-24)**

b) a trap sub-stage for placing each cell with unique destination address on a selected output of the plurality of outputs and aging each cell having a non-unique destination address; **(Cooperman teaches a system that improves existing switching**

architectures like that of A. Huang's by replacing the trap sub-network with a merged buffer architecture as shown in Cooperman's Figure 5. Cooperman's switching system routes each cell having a unique destination address to the appropriate output while aging each cell having a non-unique address. Cooperman teaches the immediate routing of cells with unique destination address to a non-busy output port in Figure 7 which is the case with cell 1 having a unique address of output 3 and is being routed to output 3 in the same time slot. See Cooperman Column 7, Lines 29-62)

c) wherein, in a next time slot, the trap sub-stage will place the aged cells on selected outputs of the plurality of outputs if the non-unique destination address for the aged cells become unique in that time slot. **(In Cooperman's switching system the aged cells with non-unique destination address are routed in the next time slot. As shown in Figure 7, cells 2 and 3 have a non-unique address of output 1 and consequently cell 1 is routed to output 1 and cell 2 is aged by misrouting it to a non-busy merged buffer. Cell 2 is then routed to buffer 1 in the second part of the first time slot and in the first part of the next time slot cell 2 is routed to output 1. Cell 2 was successfully routed to output 1 because the destination address of cell 2 is no longer non-unique and there is no output contention. See Column 7, Lines 29-62).**

24. Regarding **claim 20**, the modified invention of A. Huang and Cooperman as taught above disclosed the aforementioned invention including a multi-cast switching

system wherein the sub-stage is a Batcher sorter. **(See A. Huang Column 10, Line 67 and Cooperman Column 5, Lines 10-15)**

25. Regarding **claim 21**, the modified invention of A. Huang and Cooperman as taught above disclosed the aforementioned invention including a multi-cast switching system wherein the trap substage further comprises a trap buffer in which those cells having non-unique destination addresses for the first time are aged until the next time slot. **(See Cooperman Column 6, Lines 56-62; Column 7, Lines 29-62; In Figure 7, cells 2 and 3 have a non-unique address of output 1 and consequently cell 1 is routed to output 1 and cell 2 is aged by misrouting it to a non-busy merged buffer. Cell 2 is then routed to buffer 1 in the second part of the first time slot and in the first part of the next time slot cell 2 is routed to output 1. Cell 2 was successfully routed to output 1 because the destination address of cell 2 is no longer non-unique and there is no output contention.)**.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patent is cited to show the state of the art for copy network for multicast packet switching:

U. S. Patent (4, 813, 038) to Lee

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571 272 3088. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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HM
03-09-2005

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